## REMARKS

Applicant has carefully studied the outstanding Official Action. The present amendment is fully responsive to all points of rejection and the application is in condition for allowance. Independent claims 1and 14 are amended, claims 3 and 15 are cancelled without prejudice, claims 23 and 24 are withdrawn, and new dependent claims 33-37 are added. Favorable reconsideration and allowance of the present application are requested.

The Office Action objected to the specification of the present application as having a title which is not descriptive. Applicant has, accordingly, amended the title from: SYSTEM FOR SHIELDING INTEGRATED CIRCUITS to: METHOD ~~SYSTEM~~ FOR SHIELDING INTEGRATED CIRCUITS. As the Office Action pointed out, the claims are directed to a method of making a semiconductor device. The amendment is supported, inter-alia, by the originally filed claims. The objection to the title is deemed overcome.

The drawings stand objected to under 37 CFR 1.83(a) "because they fail to show 'a first portion of an additional layer', 'a second portion of an additional layer', 'a first integrated circuit', and 'a second integrated circuit' as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP §608.02(d)."

Regarding the alleged absence of 'a first portion of an additional layer', and 'a second portion of an additional layer', Applicant respectfully calls attention to page 14, lines 5 - 6 (referring to Fig. 1) of the application in the published PCT format, which explicitly states: "**The additional layer** 120 includes both a **non-conductive portion** 125 and **a conductive portion** 130 defining a conductive path". Applicant respectfully points out that both the specification and (at least) Fig. 1 have an additional layer which is described and depicted as having two portions.

Regarding the alleged absence of 'a first integrated circuit', and 'a second integrated circuit', Applicant respectfully points out that each of Figs. 1 - 7B (inclusive) depicts a portion of an integrated circuit. Further, Applicant refers to claim 7, which recites: "wherein the first portion of each integrated circuit has a

shape, and, for at least a first integrated circuit and a second integrated circuit of the plurality of integrated circuits, the shape of the first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit". Applicant further respectfully refers to Figs. 7A and 7B, "FIGS. 7A and 7B are simplified pictorial illustrations depicting alternative preferred patterns of the conductive portion of the protective layer of the integrated circuit of FIG. 1" (cited from the Brief Description of the Drawings). Applicant posits that a person of average skill in the art would have no difficulty seeing that Figs. 7A and 7B are, as described, different patterns (i.e. a different shape), and may be either on the same integrated circuit, or, alternatively, may just as well comprise 'a first integrated circuit', and 'a second integrated circuit'.

In light of the above discussion, the objections to the drawings are deemed overcome.

Dependent claims 6, 13, 17, and 22 stand rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. To the contrary, each of those dependent claims incorporates all of the limitations of the independent claims from which it depends. Therefore, those dependent claims particularly point out and distinctly claim the subject matter to at least the same extent as the independent claims from which they depend. The Office Action erroneously suggested that process limitations do not count. This is wrong. "Each element contained in a patent claim is deemed material to defining the scope of the patented invention...." *Warner-Jenkinson Co. v. Hilton Davis Chemical Co.*, 520 U.S. 17, 29 (1997). "A product-by-process claim, which is a product claim that defines the claimed product in terms of the process by which it is made, is proper." MPEP §2173.05(p) [citations omitted]. This was confirmed as recently as 18 May 2009 in an en banc decision of the the Federal Circuit.

*Abbott Laboratories v. Sandoz, Inc.*, 90 U.S.P.Q.2d 1769 (Fed. Cir. 2009).

Claims 6, 13, 17, and 22 are therefore deemed allowable.

*Set of Claims 1 - 5*

Claims 1, and 3 - 5 stand rejected under 35 USC §102(b) as being unpatentable over US 6,495,919 to Farrar (hereinafter, Farrar).

Claim 1 recites, in part: "depositing, over substantially **all** of an exposed surface of the integrated circuit, an additional layer of material whose conductivity can be altered;" (emphasis added). The cited portion of claim 1 is rejected over item 14 in the figures of Farrar.

Applicant respectfully points out that, in fact, the item in Farrar whose conductivity can be altered is item 12. See, for instance, Col. 4, lines 52 - 63 (emphasis added):

> If substrate 12 is not doped, doping of substrate 12 can occur simultaneously with forming an interconnect in the region within and below etch hole 26. For example if substrate 12 is monocrystalline silicon, n-doping or p-doping can be performed by implanting selected ions. **The ions that are implanted within substrate 12 will make that portion of substrate 12 into electrically conductive region 24**. For example, aluminum ions produce n-doping in a monocrystalline silicon substrate, and subsequent aluminum ion implantation, or another selected metal ion, will form implanted interconnect 30.

Regardless of whether "an additional layer of material whose conductivity can be altered" of the present invention corresponds to Farrar item 12 or Farrar item 14, Farrar, at no point, discloses that the substrate 12 is deposited "over substantially **all** of an exposed surface of the integrated circuit".

Claim 1 is therefore deemed allowable, in light of the above discussion.

Additionally, Farrar recites (col. 4, lines 63 - 64): "Although substrate 12 is usually made of monocrystalline silicon, other substrates can be provided and doped simultaneously with formation of implanted interconnect 30. By way of example, semiconductors are fabricated from compounds made by a combination of elements from periodic table groups IA-VIIA, IIA-VIA, and IIIA-VA, as well as IA-IIIA-$VI_2$ A, and IIA-IVA-$V_2$."

Since the present specification explicitly recites "the added layer may be made of polycrystalline silicon," (page 10, line 5 in the published PCT format) new claim 33, which explicitly recites "the additional layer is made of polycrystalline silicon" has been added.

Regarding claim 3, the examiner rejected claim 3 on the basis of Farrar Figs. 5 and 6, and related texts. Since claim 3 recites that "the sub-circuit is not visually distinguishable from a second portion of the additional layer, the second portion being disjoint from the first portion", one would expect to see, in Figs. 5 and 6 that the "the sub-circuit is not visually distinguishable from a second portion of the additional layer". The feature is not present in the Figures. The related text (Farrar, 4:40 - 6:44) is quoted below:

> FIG. 5 illustrates the result of ion-implantation within the section-line 5--5 in FIG. 4. In FIG. 5 an implanted interconnect 30 is illustrated wherein ions have been implanted within dielectric layer 14. A portion of implanted interconnect 30 overlaps into substrate 12. The overlap portion is implanted to overlap depth 32 that minimizes the electrical resistance interface and the thermal stress interface between interconnect 30 and electrically conductive region 24 if it is present. Preferably, implanted interconnect 30 will have a length in a range from about 1,000 to about 30,000 .
>
> Formation of an active area simultaneously with formation of an interconnect makes the active area and the interconnect self-aligned. If substrate 12 is not doped, doping of substrate 12 can occur simultaneously with forming an interconnect in the region within and below etch hole 26. For example if substrate 12 is monocrystalline silicon, n-doping or p-doping can be performed by implanting selected ions. The ions that are implanted within substrate 12 will make that portion of substrate 12 into electrically conductive region 24. For example, aluminum ions produce n-doping in a monocrystalline silicon substrate, and subsequent aluminum ion implantation, or another selected metal ion, will form implanted interconnect 30.
>
> Although substrate 12 is usually made of monocrystalline silicon, other substrates can be provided and doped simultaneously with formation of implanted interconnect 30. By way of example, semiconductors are fabricated from compounds made by a combination of elements from periodic table groups IA-VIIA, IIA-VIA, and IIIA-VA, as well as IA-IIIA-$VI_2$ A, and IIA-IVA-$V_2$.

Implanted overlap depth 32 expands laterally upon heat treatment of device 10 to form, for example, an active area in a transistor source-drain structure.

Dielectric layer 14 can be selected to be an organometallic dielectric or equivalent that releases metal elements in favor of bonding with oxygens or nitrogens and equivalents. Treatment is carried out in an oxygen or nitrogen atmosphere following implantation. Implantation of metal ions to form implanted interconnect 30 or an implanted thermal conductor will, either spontaneously or with heat treatment, cause the metals in the organometallic dielectric to combine with the implanted metal ions to form a substantially coherent and continuous metal interconnect.

Combination of the metals in the organometallic and the implanted species accomplishes more metallization in the implanted interconnect 30 or in an implanted thermal conductor than simple implantation alone achieves. Combination also renders the organometallic dielectric that remains more resistant to electrical conductivity than regions not implanted with metal ions.

An alternative to an organometallic dielectric that releases its metal element in favor of oxides or nitrides, is an organometallic that releases its metal element by catalysis caused by the presence of the implanted metal species. By this optional method, the regions of dielectric not implanted by the metal ions, do not become conductive at the temperatures at which the catalytic reaction occurs.

FIG. 6 illustrates electrically conductive region 24 that is imbedded within substrate 12. Ion implantation into dielectric layer 14 is illustrated as implanted interconnect 30, extending to implanted overlap depth 32. Overlap depth 32 can be optimized so as to minimize the electrical resistance interface and the thermal stress interface between interconnect 30 and electrically conductive region 24. Implanted overlap depth 32 and implanted interconnect 30 form a substantially continuous electrically conductive interface between substrate 12 and implanted interconnect 30. The advantage of a substantially continuous electrical interface between an interconnect and an electrically conductive region is that both resistivity and thermal stresses are ameliorated for field use of the semiconductor device.

The portion of Farrar cited in the Office Action fails to disclose that "the sub-circuit is not visually distinguishable from a second portion of the additional layer". Indeed, Farrar does not deal with the visibility or lack thereof of any of the components of his integrated circuit.

Accordingly, claim 1 has been amended to recite the limitation of claim 3, in order to make the distinction between claim 1 as amended and Farrar especially clear.

Claim 1 is therefore deemed allowable.

Claim 3 has been cancelled without prejudice.

Claims 4 and 5 depend from claim 1, and recite additional patentable material.

Claim 4 and 5 are therefore deemed allowable in light of the above discussion of the allowability of claim 1.

Claim 2 stands rejected under 35 USC §103(a) as being unpatentable over Farrar in view of US 4,339,285 to Pankove.

Claim 2 depends from claim 1, and recites additional patentable material.

Claim 2 is therefore deemed allowable in light of the above discussion of the allowability of claim 1.

*Set of Claims 7 - 12*

Claims 7 - 8, and 10 - 13 stand rejected under 35 USC §102(b) as being unpatentable over Farrar.

Claim 7 recites, in part: "selectively altering the conductivity of a first portion of the additional layer by selective annealing, to produce a sub-circuit in the additional layer, the sub-circuit being in operative electrical communication with the integrated circuit". The Office Action cited Farrar, Figs. 3 - 5, and related texts with respect to this limitation.

Applicant submits that since the limitation of claim 7 recites that the first portion of the additional layer is selectively altered by selective annealing, and Farrar does not recite any selective altering or selective annealing, the rejection of claim 7 under 35 USC §102(b) is an improper rejection.

Furthermore, the conclusion of claim 7 recites: "wherein the first portion of each integrated circuit has a shape, and, for at least a first integrated circuit and a second integrated circuit of the plurality of integrated circuits, the shape of the first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit." The Office Action erroneously

asserted that these features of claim 7 are recited in Farrar, at least Figs. 5 - 8 and related texts. To the contrary, Farrar does not disclose "the first portion of each integrated circuit has a shape"; "a first integrated circuit and a second integrated circuit"; and "the shape of the first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit".

In that several significant features of claim 7 are not described at all in Farrar, the rejection of claim 7 is overcome.

Claim 7 is therefore deemed allowable.

Claim 8 recites: "the shape of the first portion of each one of the plurality of integrated circuits on a production wafer is different from the shape of the first portion of any other of the plurality of integrated circuits on the production wafer."

The Office Action rejected claim 8 in view of the description of Farrar Fig. 8 and related texts. The description of Farrar Fig. 8 (5:60 - 6:44) is quoted below:

> FIG. 8 is an illustration of semiconductor device 10 with three (3) features of the present invention illustrated therein. Two implanted interconnects 30 are illustrated wherein implantation has occurred in a first instance above electrically conductive region 24, and in a second instance above substrate 12 with no electrically conductive region thereunder. Implanted thermal conductor 36 is also illustrated in FIG. 8 wherein no electrical connection is made to substrate 12. Metallization lines 38 have been formed upon upper surface 34 of dielectric layer 14. Implanted interconnects 30 form interconnects from to metallization lines 38 to electrically conductive region 24 and to substrate 12. Implanted thermal conductor 36 lies beneath metallization lines 38 and serves as an excess Joule heat collector for metallization lines 38.
>
> Preferred ions to form the implanted interconnect are chosen to be compatible with the structure in which it is used. In an integrated circuit, implantation of copper or gold in areas where these elements might migrate into the substrate could cause field failure and affect carrier lifetime. In other applications, copper or gold would be acceptable materials to use. In a semiconductor application, elements such as Al, Ni, Cr, Mo, Ta, W, Ti, Zr, Hf, or V and equivalents might be chosen. In some applications in which a preferred dielectric layer material is used, Ni would be a preferred element because of its resistance to oxidation and its relatively good electrical conductivity. In some applications in which a preferred dielectric layer material is used, Al would be a preferred element

> because it can be implanted into a dielectric that will not substantially oxidize it and because of aluminum's relatively good electrical conductivity.
>
> Materials that will form the implanted interconnect or thermally conductive implants are selected so that when the total implant dose is integrated over any segment, the total amount of implant meets or exceeds the desired concentration. In an example of a 10,000 film the first implant dose is selected so that at least 4 percent of the implant dose penetrates the entire 10,000 film, and that at least 10 percent of the implant dose is deposited in the 500 slice between 9,500 and 10,000 . The percentage of the implant dose is then calculated for each succeeding slice of 500 in which any appreciable amount of the implant dose is absorbed. The dose of the implant is then calculated to produce a concentration that exceeds the desired minimum in the first slice. The percentage is then multiplied by the dose amount and divided by the nominal Si concentration of about 5.times.10.sup.22 atoms/cm.sup.3 to obtain the percent of the implanted species in each slice. The second and succeeding implants are determined in a like manner until an implanted interconnect or an implanted thermal conductor is formed as desired.

To summarize the description of Farrar, Fig. 8, the disposition of the two implanted interconnects, the thermal conductor, metallization lines is described. Then a list of elements which are appropriate to form the interconnect and the thermally conductive implants is presented. Finally, the concentration of said elements is discussed.

What is missing, however, from the description of Farrar, Fig. 8 is:

a discussion of "the shape of the first portion of each one of the plurality of integrated circuits";

a discussion of "a production wafer"

a discussion of how the shape of the aforementioned first portion "is different from the shape of the first portion of any other of the plurality of integrated circuits on the production wafer."

In short, Farrar Fig. 8 does not disclose any of the elements of claim 8.

Claim 8 also depends from claim 7 and recites additional patentable material.

Claim 8 is therefore deemed allowable in light of the above discussion, as well as the discussion of the allowability of claim 7.

Regarding the rejection of claim 10, Applicant refers to the discussion of the allowability of claim 3 (presently amended to be recited as a limitation of claim 1) above. Claim 10 also depends from claim 7 and recites additional patentable material.

Claim 10 is therefore deemed allowable in light of the above discussion of the allowability of claim 3 (presently amended to be recited as a limitation of claim 1), as well as the discussion of the allowability of claim 7.

Claims 11 and 12 depend from claim 7 and recite additional patentable material.

Claims 11 and 12 are therefore deemed allowable in light of the above discussion of the allowability of claim 7.

Claim 9 stands rejected under 35 USC §103(a) as being unpatentable over Farrar in view of Pankove.

Claim 9 depends from claim 7 and recites additional patentable material.

Claim 9 is therefore deemed allowable in light of the above discussion of the allowability of claim 7.

*Set of Claims 14 - 16*

Claims 14 - 16 stand rejected under 35 USC §102(b) as being unpatentable over Farrar.

As per the discussion of claim 1 above, Farrar does not disclose that the substrate 12 is deposited "over substantially **all** of an exposed surface of the integrated circuit".

In addition, as was discussed above regarding claim 3 (presently amended to be recited as a limitation of claim 1) above, the limitation of claim 15, "the sub-circuit is not visually distinguishable from a second portion of the additional layer, the second portion being disjoint from the first portion" is not disclosed in Farrar.

In order to stress the distinction of independent claim 14 over Farrar, the limitation of claim 15 has been amended into claim 14, and claim 15 has been cancelled without prejudice.

Amended claim 14 is therefore deemed allowable.

Claim 16 depends from claim 14 and recites additional patentable material.

Claim 16 is therefore deemed allowable in light of the above discussion of the allowability of amended claim 14.

*Set of Claims 18 - 22*

Claims 18 - 22 stand rejected under 35 USC §102(b) as being unpatentable over Farrar.

Claim 18, in part, recites: "for each one of the plurality of integrated circuits, selectively doping only a first portion of the additional layer of material of the one integrated circuit"

Farrar describes (col. 4, lines 30 - 35, cited by the Examiner): "The step of ion implantation may serve as both a doping step in forming an electrically conductive region in substrate 12, and as an interconnect-forming implantation step of the present invention. In this simultaneous doping and interconnect-forming method alternative, an extra process step is avoided for active region doping."

Farrar does not describe "selective doping of only a first portion of the additional layer of material of the one integrated circuit". Rather Farrar is describing a method to simultaneously dope and form the interconnect, thereby avoiding an extra process step.

Furthermore, the conclusion of claim 18, similar to claim 7, recites: "wherein the first portion of each integrated circuit has a shape, and, for at least a first integrated circuit and a second integrated circuit of the plurality of integrated circuits, the shape of the first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit." The Office Action erroneously asserted that these features of claim 18 are recited in Farrar, at least Figs. 5 - 8 and related texts. To the contrary, Farrar does not disclose "the first portion of each integrated circuit has a shape"; "a first integrated circuit and a

second integrated circuit"; and "the shape of the first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit".

Additionally, the other arguments against the rejection of claim 7, discussed above, apply as well to claim 18.

Claim 18 is therefore deemed allowable, in light of the above discussion, as well as the discussion of the allowability of claim 7.

Claim 19 depends from claim 18 and recites additional patentable matter. Additionally, claim 19 corresponds to claim 8, and therefore the discussion above concerning the rejection of claim 8 applies as well to claim 19.

Claim 19 is therefore deemed allowable with reference to the above discussion of the allowability of claim 18, as well as the above discussion of the allowability of claim 8.

Claim 20 recites that the sub-circuit is not visibly distinguishable from a second portion of the additional layer.

Claim 20 depends from claim 18 and recites additional patentable matter. Furthermore, the allowability of a claim reciting an object being not visibly distinguishable from its environment is discussed above, with reference to the allowability of claim 3 (presently amended to be recited as a limitation of claim 1).

Claim 20 is therefore deemed allowable with reference to the above discussion of the allowability of claim 18, as well as the above discussion of the allowability of claim 3 (presently amended to be recited as a limitation of claim 1).

Claim 21 depends from claim 18 and recites additional patentable matter.

Claim 21 is therefore deemed allowable with reference to the above discussion of the allowability of claim 18.

*Set of Claims 25 - 32*

Claims 25 - 26, and 28 - 32 stand rejected under 35 USC §102(b) as being unpatentable over Farrar.

As with claims 1 and 14, Farrar does not disclose that the substrate 12 is "disposed over substantially **all** of a surface of the lower integrated circuit portion".

Claim 25 further recites: "the sub-circuit being not visually distinguishable from a second portion of the additional layer, the second portion being disjoint from the first portion". As has been discussed above with reference to claim 3 (presently amended to be recited as a limitation of claim 1), the feature of one portion not being visually distinguishable from a second portion in the integrated circuit of the present invention is not disclosed in Farrar.

Claim 25 is therefore deemed allowable, with reference to the above discussion of the allowability of clam 1 and claim 3 (presently amended to be recited as a limitation of claim 1).

Claim 26 recites: "depositing, over substantially **all** of an exposed surface of the lower integrated circuit portion". The issue of Farrar's not disclosing such a feature has been discussed above with reference to claim 1, claim 14, and claim 25.

Claim 26 further recites: "selectively altering the conductivity of a first portion of the additional layer by selective annealing". The issue of selective annealing has been discussed above, at least, with reference to Claim 7.

In addition, claim 26 depends from claim 25, and recites additional patentable subject matter.

Claim 26 is therefore deemed allowable in light of the discussions of the allowability of claims 1, 7 and 25.

Regarding claim 28, the Office Action did not describe any portion of Farrar which discloses "the selectively altering comprises altering substantially without removing any part of the additional layer".

In addition, claim 28 depends from claim 26, and recites additional patentable subject matter.

Claim 28 is therefore deemed allowable in the absence of any specific rejection of claim 26 vis-à-vis Farrar, and in view of the above discussion of the allowability of claim 26.

In addition, new claims 34 - 37 have been added reciting the limitation of claim 28 as depending, respectively, from claims 1, 7, 14, and 18.

Claim 29 recites the features of: "depositing over substantially **all** of an exposed surface...";

"selectively doping: and

"selectively altering".

These features and limitations have all been discussed throughout this response, with reference, at least, to the allowability of claims 1 and 7.

In addition, claim 29 depends on claim 25, and recites additional patentable subject matter.

Claim 29 is therefore deemed allowable with reference to the allowability of claims 1, 7, and 29.

Claims 30 and 32 depend on claim 25, and recites additional patentable subject matter.

Claims 30 and 32 are therefore deemed allowable with reference to the allowability of claim 25.

Claim 31, similar to claim 7, recites: "wherein the first portion has a shape, and, for at least a first integrated circuit and a second integrated circuit of the plurality of integrated circuits on a production wafer, the shape of the first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit." The Office Action erroneously asserted that these features of claim 31 are recited in Farrar, at least Figs. 7 - 8 and related texts. To the contrary, Farrar does not disclose "the first portion of each integrated circuit has a shape"; "a first integrated circuit and a second integrated circuit"; and "the shape of the first portion of the first integrated circuit is different from the shape of the first portion of the second integrated circuit".

Additionally, claim 31 depends on claim 25, and recites additional patentable subject matter.

Claim 31 is therefore deemed allowable with reference to the allowability of claim 25.

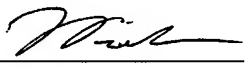
Claim 27 stands rejected under 35 USC §103(a) as being unpatentable over Farrar in view of Pankove.

Claim 27 depends from claim 26 and recites additional patentable material.

Claim 27 is therefore deemed allowable in light of the above discussion of the allowability of claim 26.

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance. Favorable reconsideration and allowance of the present application are respectfully requested.

Respectfully submitted,



1 July 2009

L. Friedman
Reg. No. 37,135

HUSCH BLACKWELL SANDERS LLP
WELSH & KATZ
120 South Riverside Plaza, Suite 2200
Chicago, Illinois 60606
(312) 655-1500